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APPLICATION NO. FILING DATE FIRST NAMED INVENTOR ATTORNEY DOCKET NO. CONFIRMATION NO. 10/086,197 03/01/2002 Sanjiv Garg 097749182047.0170009 1234 EXAMINER 11/25/2003 STERNE, KESSLER GOLDSTEIN & FOX DONAGHUE, LARRY D 1100 NEW YORK AVENUE, N.W. ART UNIT WASHINGTON, DC 20005 PAPER NUMBER 2154 DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.





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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,197	03/01/2002	Sanjiv Garg	097749182047.0170009	1234
22887 75	590 08/28/2003			
DISCOVISIO	N ASSOCIATES		EXAM	NER
	AL PROPERTY DEVELO REET, SUITE 200	PMENT	DONAGHUE	, LARRY D
IRVINE, CA	92614		ART UNIT	PAPER NUMBER
			2154	8
			DATE MAILED: 08/28/2003	0

Please find below and/or attached an Office communication concerning this application or proceeding.

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	Application No.	Applicant(s)		
Office Action Summary	Examiner		Group Art Unit	
—The MAILING DATE of this communication appears	s on the cover sh	eet beneath the co	rrespondence addr	ess—
Period for Reply		>		
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO OF THIS COMMUNICATION.	EXPIRE	MONTH(S)	FROM THE MAILIN	G DATE
 Extensions of time may be available under the provisions of 37 CFR 1. from the mailing date of this communication. If the period for reply specified above is less than thirty (30) days, a reperiod NO period for reply is specified above, such period shall, by default, experience to reply within the set or extended period for reply will, by statute. 	oly within the statutory expire SIX (6) MONTH	minimum of thirty (30) o	days will be considered ties of this communication.	
Status	, ,			
Responsive to communication(s) filed on This action is FINAL.	es No.	5-7	<u> </u>	·
 Since this application is in condition for allowance except f accordance with the practice under Ex parte Quayle, 1935 			the merits is closed	in
Disposition of Claims				
Z - Z - Z - Z - Z - Z - Z - Z - Z - Z -		is/are p	ending in the applica	tion.
Of the above claim(s)		is/are w	vithdrawn from consid	deration.
□ Claim(s)	-	is/are a	ıllowed.	
☐ Claim(s) 2 - 2 ©		is/are re	ejected.	
□ Claim(s)		is/are o	bjected to.	
□ Claim(s)			eject to restriction or e	election
Application Papers		•		
☐ See the attached Notice of Draftsperson's Patent Drawing				
☐ The proposed drawing correction, filed on	• •	• •	i.	
☐ The drawing(s) filed on is/are objecte	ed to by the Exami	ner.		
 The specification is objected to by the Examiner. The oath or declaration is objected to by the Examiner. 				
Priority under 35 U.S.C. § 119 (a)-(d)		•		
☐ Acknowledgment is made of a claim for foreign priority und	dor 35 11 8 C & 11	0(a) (d)		
 □ All □ Some* □ None of the CERTIFIED copies of the received. □ received in Application No. (Series Code/Serial Number received in this national stage application from the Interest.) 	ne priority docume	nts have been		
•	·			
*Certified copiés not received:			•	
Attachment(s)	S		DTO 145	
Information Disclosure Statement(s), PTO-1449, Paper No	o(s).	☐ Interview Summ	•	DTC :
□ Notice of Reference(s) Cited, PTO-892			al Patent Application	
☐ Notice of Draftsperson's Patent Drawing Review, PTO-948	I	⊔ Other		·
Office	Action Summary			

Art Unit: 2154

- 1. Claims 2-20 are presented for examination.
- 2. Claim 1 has been canceled at the request of applicant.
- 3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 2-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims of U.S. Patent No. 5,737,624. Although the conflicting claims are not identical, they are not patentably distinct from each other because The claims of 5,737,624 set forth a system which is an obvious variation of claim 2 of the instant application system for register renaming in a computer system capable of out-of-order instruction

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execution (claim 1, lines 1-2), comprising: a temporary buffer comprising a plurality of storage

locations for storing execution results (claim 13, lines 2-4), wherein an execution result for an

instruction in an instruction window is stored in one of said plurality of storage locations (claim

13, lines 2-4), said one of said plurality of storage locations being assigned to said instruction in

said instruction window(claim 13, lines 2-7); and tag assignment logic that outputs a tag

comprising a temporary buffer storage location address in place of a register address for an

operand of a first instruction claim 13, lines 5-13), wherein said temporary buffer storage location

address is an address of said operand in one of said plurality of storage locations if said first

instruction is dependent on a previous one of said plurality of instructions in said instruction

window for said operand (claim 13, lines 8-13).

5. Garg et al. was cited by examiner on paper no. 4.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section

122(b) only if the international application designating the United States was published under Article 21(2)(a)

of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

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7. Claims 2-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Nguyen et al. (5,448,705).

Nguyen et al. was cited by examiner on paper no. 4.

- 8. Nguyen taught the invention (claim 13) as claimed including a computer system (100), comprising: a memory unit for storing program instructions (132, 110, 112); a bus coupled to said memory unit for retrieving said program instructions (114, 136); and a processor (104) coupled to said bus, wherein said processor comprises a register renaming system (496), comprising: a temporary buffer comprising a plurality of storage locations for storing execution results (552), wherein an execution result for an instruction in an instruction window is stored in one of said plurality of storage locations, said one of said plurality of storage locations being assigned to said instruction in said instruction window; and tag assignment logic that outputs a tag comprising a temporary buffer storage location address in place of a register address for an operand of a first instruction if said first instruction is dependent on a previous one of said plurality of instructions in said instruction window for said operand, wherein said temporary buffer storage location address is an address of said operand in one of said plurality of storage locations (col. 37, line 1 col. 38, line 12).
- 9. As to claim 9, Nguyen et al. taught said processor further comprises termination logic that transfers said execution results in said plurality of storage locations in said temporary buffer to register file locations in-order based on the order of instructions in said instruction window (col. 37, lines 53-63).

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- 10. As to claim 10, Nguyen et al. taught said termination logic transfers a plurality of execution results from said temporary buffer to said register file simultaneously (col. 37, lines 53-63).
- 11. As to claim 11, Nguyen et al. taught said termination logic transfers an execution result for an instruction from said temporary buffer to said register file when all execution results for all prior instructions are retireable (col. 37, lines 53-63).
- 12. As to claim 12, Nguyen et al. taught said tag further comprises an identifier that indicates whether said address within said tag is an address within a register file or said plurality of storage locations (col.36, lines 58-68).
- 13. As to claim 13, Nguyen et al. taught said processor further comprises register file port multiplexers that pass said tag to read address ports of said temporary buffer for accessing said execution results (col. 36, lines 35-63).

As to claims 2-12 and 14-20 fail to teach above or beyond claims 8-13, and is reject for the reason set forth, above.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

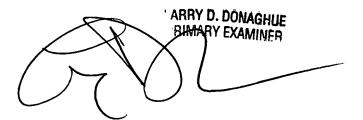
Art Unit: 2154

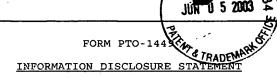
MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to L. Donaghue whose telephone number is (703) 305-9675. The examiner can normally be reached on M-F from 8:00 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An, can be reached on (703) 305-9678. The fax phone number for an official fax is (703) 746-7238, an after-final fax is 703-746-7238 and a draft or non-official fax is 703-746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.





ATTY. DOCKET NO. A 2047.0170009 (As Corrected) 1

APPLICATION NO. 10/086,197

APPLICANT GARG et al.

FILING DATE March 1, 2002 GROUP 2154

DOCUMENT DATE NAME CLASS SUB-CLASS FILING DATE						March 1, 2002	2154		
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AB1 4.875,806 06/1987 Uchida AC1 4,722,049 01/1988 Lahti AD1 4.807,115 02/1999 Tong AE1 4,901,233 02/1990 Uplay AF1 4,903,196 02/1990 Pomerene et al. AG1 4,942,525 07/1990 Shintaril et al. AG1 4,942,525 07/1990 Shintaril et al. AH1 4,992,938 02/1991 Cocke et al. AH1 5,067,069 11/1991 File et al. FOREIGN PATENT DOCUMENTS XAMINER OCCUMENT NUMBER 11/1992 EP AK1 0 533 337 A1 03/1993 EP AK1 0 533 337 A1 03/1993 EP AK1 0 533 337 A1 12/1991 PCT OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AM 1 Acosta, R. D. et al., "An Instruction Issuing Approach to Enhancing Performance in Multiple Functional Unit Processors," IEEE Transactions On Computers, IEEE, Vol. C-35, No. 9, September 1986, pp. 815-828. AN 1 Agenvala, T. and Cocke, J., High Performance Reduced Instruction Set Processors, IBM Research Division, March. 1987, pp. 1-61. AB AB 1 4, "Single Instruction Stream Parallelism Is Greater Than Two," 18th Annual Intermational Symposium on Programming, Springer, ISBN 3-640-19027-9, 1988, pp. 221-235.	XAMINER NITIAL				DATE	NAME	CLASS		FILING DATE
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant. ::ODMA\MHODMA\SKGF_DC1;126875;1

FORM PTO-1449 INFORMATION DISCLOSURE

APPLICATION NO. ATTY. DOCKET NO. 2047.0170009 (As Corrected) 10/086,197

APPLICANT GARG et al.

					FILING DATE March 1, 2002		GROUP 2154		
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	AA2	5,109	9,495	04/1992	Fite et al.				
	AB2	5,142	2,633	08/1992	Murray et al.		<u> </u>		
	AC2	5,214	1,763	05/1993	Blaner et al.				
	AD2	5,222	2,244	06/1993	Carbine et al.				
	AE2	5,226	6,126	07/1993	McFarland et al.				
	AF2	5,230	0,068	07/1993	Van Dyke et al.	•			
	AG2	5,251	1,306	10/1993	Tran				
b-	AH2	5,261	1,071	11/1993	Lyon				
THE	Al2	5,345	5,569 ⁻	09/1994	Tran				
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9	AN	2	Conference		Architecture for a Trace Schedul Support for Programming Langua				
م	AO	2			ole, Out-of-Order, Instruction Issu entation Services, August 1991, p			alar Process	<i>ors</i> , Dissertation f
	AP	2			.M., "Percolation of Code to Enh IEEE, December 1972, pp. 141		spatching	and Execut	ion," <i>IEEE</i>
	AQ	2			ntation of Prolog via VAX 8600 M ual Workshop on Microprogramm	ning, ACM, 1986	, pp. 68-7	74.	n Microarchitectu
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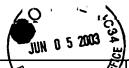
ATTY. DOCKET NO. 2047.0170009 (As Corrected)

APPLICATION NO. 10/086,197

APPLICANT GARG et al.

FILING DATE March 1, 2002

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	AA3	5,35	5,457	10/1994	Shebanow et al.		1		1		
77	AB3	5,39	8,330	03/1995	Johnson		1				
	AC3		2,757	08/1995	McFarland et al.			\neg			
	AD3	1	3,705	09/1995	Nguyen et al.						
1	AE3	1	7,156	01/1996	Popescu et al.	`	$\neg \uparrow$				<u></u>
	AF3	+ -	7,499	03/1996	Garg et al.						
1	AG3		1,776	10/1996	Popescu et al.				.		
1'_	AH3		4,927	11/1996	Scantlin	·	7			 	+
7	AI3	1	2,636	01/1997	Popescu et al.		- 1			1	
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9	AM	<u>3</u>			"Code Scheduling and Register A on Supercomputing, ACM, 1988,			asic B	Blocks	s," <i>Pr</i> c	oceedings of the
9	AM AN	3	2nd Internation Gross, T.R. a	and Hennessy, J		pp. 442-452.		- 15			- J
9			Gross, T.R. a Microprogran Groves, R.D.	and Oehler, R.,	on Supercomputing, ACM, 1988, .L., "Optimizing Delayed Branches	pp. 442-452. s," Proceeding 20.	gs of the	he 5th	Annu	ual Wo	orkshop on ngs 1989 IEEE
9 9	AN	3	Gross, T.R. a Microprogram Groves, R.D. International	and Oehler, R., Conference on C	on Supercomputing, ACM, 1988, L., "Optimizing Delayed Branches, CM, October 5-7, 1982, pp. 114-1 "An IBM Second Generation RISC	pp. 442-452. s," Proceeding 20. C Processor A ters and Proce	gs of the	cture,	Annu " Pro E, Oc	ceedir	orkshop on ngs 1989 IEEE 1989, pp. 134-13
9 9 9	AN	<u>3</u>	Gross, T.R. a Microprogram Groves, R.D. International Horst, R.W. e International	and Hennessy, J. nming, IEEE & A and Oehler, R., Conference on C et al., "Multiple In Symposium on C	on Supercomputing, ACM, 1988, L., "Optimizing Delayed Branches, CM, October 5-7, 1982, pp. 114-1 "An IBM Second Generation RISC Computer Design: VLSI in Computer Design:	pp. 442-452. s," Proceeding 20. C Processor A ters and Proce yclone Proces 0, pp. 216-226 and Analysis, 0. 282-291.	gs of the Architeessors assor," F	cture,	Annu" Process, Oc	ceedir tober s of th	orkshop on ngs 1989 IEEE 1989, pp. 134-13 e 17th Annual
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ATTY. DOCKET NO. 2047.0170009 (As Corrected)

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	AA4	5,625	5,837	04/1997	Popescu et al.				1	
1	AB4	5,627	7,983	05/1997	Popescu et al.				1	
	AC4	5,708	3,841	01/1998	Popescu et al.					
	AD4	5,737	7,624	04/1998	Garg et al.					
	AE4	5,768	3,575	06/1998	McFarland et al.					
	AF4	5,778		07/1998	Henstrom et al.		\neg			
	AG4	5,797		08/1998	Popescu et al.		1	+	!	
	AH4	5,832		11/1998	Kelly et al.		\neg	_	†	
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9			Hwu, W. and Hawaii Inten	d Patt, Y.N., "Des national Conferen	IEEE, Vol. C-36, No. 12, Decemb	rocessor Chip, o. 330-336.	96-15	edings	of the	Twentieth Annual
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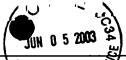
APPLICANT GARG et al.

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3	AA5	5,97	4,526	10/1999	Garg et al.				
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2	AM	<u>5</u>	IBM Journa	l of Research and	f Development, IBM, Vol. 34, N	No. 1, January 1990,	pp. 1-70.		
	AN	<u>5</u>	Johnson, W	'. M., Super-Scala	ar Processor Design, Dissertat	ion for Stanford Univ	ersity, 198	19, pp. ii-x	iii and 1-134.
	AO	<u>5</u>	Proceeding:	. and Wall, D.W., s - <i>3rd Internation</i> CM, April 1989, p	"Available Instruction-Level Pa al Conference on Architectura p. 272-282.	arallelism for Supers I Support for Progran	calar and a	Superpipe guages a	elined Machines," nd Operating
	АР	<u>5</u>	Jouppi, N.P Design, IEE	., "Integration and E, October 2-4, 1	l Packaging Plateaus of Proce 989, pp. 229-232.	essor Performance,"	Internation	al Confer	ence of Computer
9	AQ	5 9			m Distribution of Instruction-Letions on Computers, IEEE, Vo				
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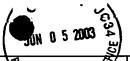
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	AN	6	Vol. 4, 1990.	, pp. 173-201. D. and Hill, G., "	eduling For Superscalar Architecture of the state of the			
			Vol. 4, 1990 Lightner, B.I Society Pres	pp. 173-201. D. and Hill, G., " ss, February 25 and Patt, Y., "Exp	The Metaflow Lightning Chip Set,"	COMPCON Spring '91	digest of pap	ers, IEEE Compu
	AO	<u>6</u>	Vol. 4, 1990 Lightner, B. E. Society Pres Melvin, S. ar Techniques, pp. 287-296. Murakami, K	pp. 173-201. D. and Hill, G., " ss, February 25 and Patt, Y., "Exp The 18th Annu. C. et al., "SIMP (rchitecture," Pro	The Metaflow Lightning Chip Set," - March 1, 1991, pp. 13-18. - Soloiting Fine-Grained Parallelism Ti	COMPCON Spring '91 nrough a Combination imputer Architecture, V	of Hardware a	ners, IEEE Compu and Software ACM, May 1991,
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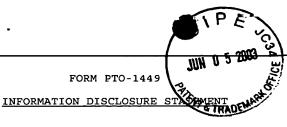
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	AN	<u>8</u>			., "The Performance Potentia Symposium on Computer Arc				," Proceedings of
	AO	<u>8</u>			A Restartable Architecture U hitecture, ACM, June 1987, p		ceedings	s of the 14th I	nternational
	AP	8	Popescu, V.	et al., "The Meta	flow Architecture", IEEE Micro	o, IEEE, June 199 [.]	1, pp. 10	-13 and 63-73	3.
	AQ	8			Beyond Static Scheduling in a . 18, Issue 3, June 1990, pp.		essor," A	ACM SIGARO	H Computer
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	AN	<u>7</u>			HPS, a Restricted Data Flow Mir , 1986, pp. 254-258.	croarchitecture for Hi	gh Performan	ce Computers,"
	AO	7	Patt, Y.N. et a	al., "HPS, A New M Microprogramming	licroarchitecture: Rationale and Ir 7, ACM, December 1985, pp. 103	ntroduction," <i>Proceed</i> -108.	lings of the 18	ith Annual
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7	ACI)		A. and Hennessy, . b. xi-xv, 257-278, 29	J.L, <i>Computer Architecture A Qua</i> 90-314 and 449.		1	aann Publishers,
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9	АМ	9			R.,"Implementation of Precise II mposium on Computer Architect				oceedings of the
	AN	9	Smith, M.D. Architectural	et al., "Limits on Support for Pro	Multiple Instruction Issue," <i>Proc</i> gramming Languages and Oper	ceedings of the Sating Systems, I	3rd Intern ACM, Ap	national Confe ril 1989, pp. 2	erence on 90-302.
	AO	9	Sohi, G. S. a Proceedings	ind Vajapeyam, of the 14 th Annu	S., "Instruction Issue Logic For lad International Symposium on	High-Performand Computer Archit	ce, Interrecture, A	ruptable Pipeli ACM, June 2-5	ned Processors," 5, 1987, pp. 27-34.
	АР	9			., "Hierarchical Registers for Sci Supercomputing, ICS, July 4-8,			ference Proce	edings: 1988
	AQ	9	Thornton, J.f	E., Design of a C	Computer: The Control Data 660	00, Control Đata	Corporat	tion, 1970, pp.	58-140.
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INFORMATION DISCLOSURE STATEMENT

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APPLICANT

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